SIES Graduate School of Technology

DepartmentOfElectronics and Telecommunication Engineering

Workshop on Digital System Design on FPGA Using Verilog

1st January 2024 to 6th January 2024

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Since their introduction in the 1985, field programmable gate arrays (FPGAs) have become increasingly important to the electronics industry. They have the potential for higher performance and lower power consumption than microprocessors and compared with ASICs, offer lower non-recurrent engineering (NRE) costs, reduced development time, easier debugging and reduced risk. Since modern FPGAs can meet many of the performance requirements of ASICs, they are being increasingly used in their place. The aim of workshop is to provide a platform for students to learn, design and implement digital system on FPGA using Verilog/VHDL.

In this course students will learn Basics of FPGA Board , FPGA Programming using Verilog.

AboutInstructors:

This course will be taught by a team of expert from SIESGSTfaculty-Electronics and TelecommunicationDepartment, along with some Industry Experts.

IndustryExpert:

Suraj Shetty, Samsung semiconductor India Research(SSIR), Senior Engineer, Design verification

Faculty Members:

1. Prof. Dr.PreetiHemnani
2. Prof. Pranavi Nikam

CourseObjectives:

• To undersatnd FPGA and HDL language
• To understand design of combinational circuit using verilog
• To understand design of sequential circuit using verilog
• To understand Test bench and simulation uisng different tools
• To understand Finite state mahine design using verilog
• To undersatnd FPGA and HDL language

CourseOutcomes:

At the end of the course, students will be able to

• Implement Verilog design using EDA and xilink platform
• Implement combinational circuits using Verilog
• Implement sequential circuits using Verilog
• Implement FSM using Verilog
• Implement hamming code , error detetction and correction using verilog

CourseContent:

Module	Contents	Hours
1.	1.1 Introduction to basics of FPGA 1.2 Introduction to Verilog coding: Data types , Constant, Parameters, Wires , Registers , operators	4hrs
2.	2.1 Continues and Procedural assignment statement 2.2 Different Modeling style : Gate level, Structural level, Behavioral Level 2.3 Programming based on different modeling style 2.4 Xilink software introduction	7hrs
3.	3.1: Implementation of combinational circuits on FPGA: Half adder , Full adder , Multiplexer, Decoder	6hrs
4	4.1 : Implementation of sequential circuits on FPGA Flip Flop, Asynchronous counter, Synchronous counter, Mod counter , Sequence detector	8 hrs
5	5.1 : FSM design 5.2: FSM implementation on FPGA	2hrs 6 hrs
6	Hamming code, Error detetction and correction using verilog on FPGA	6 Hrs
7	Designing of Projects .	15hrs

Assessment:

1. Module wise assignments and quizzes will be taken.
2. Mini Projects will be assigned in a group of 4 students.

CourseCoordinators:

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Department of Electronics & Telecommunication Engineering

Event Report

Digital System Design on FPGA using Verilog
(1/1/2024 to 6/1/2024)

Event Information
Event Type: Student Development program with Intenship
Event title: Digital System Design on FPGA using Verilog
Resource Person: Dr.Preeti Hemnani , Prof. Pranavi Nikam
Event date:1/1/2024 to 6/1/2024
Organized for: Student Faculty
Organizedby Department : Electronics & Telecommunication Engineering
Target audience :TE students **Branch: EXTC** **Number of students registered:40** **Number of students joined on first day:29** **Number of students completed the course:29** **Number of students completed the internship projects:29**
Attachments: 1. List of students with internship Projects completed by the students **2. Attendance report** **3. Feedback**

4. Certificate, Photographs (in JPEG/PNG)

Event Description

EXTC department faculties have conducted 15 days student development program followed by internship, “FPGA Design using Verilog”. Program was conducted by Prof. Pranavi Nikam and Prof. Dr. Preeti Hemnani.

Objective of the workshop was to bridge the gap between industry requirements and academic. 18 students attended the course and successfully developed and submitted project individually. Students completed their projects during online internship by SIESGST.

Prof. Sagar Mhatre from K. J somaiya Institute of Engineering , Sion has conducted one day hands on session on PYNQ Board .

Certificates were given to students on successful completion and presentation of developed applications. Feedback was collected and overall feedback shows students were satisfied with content.

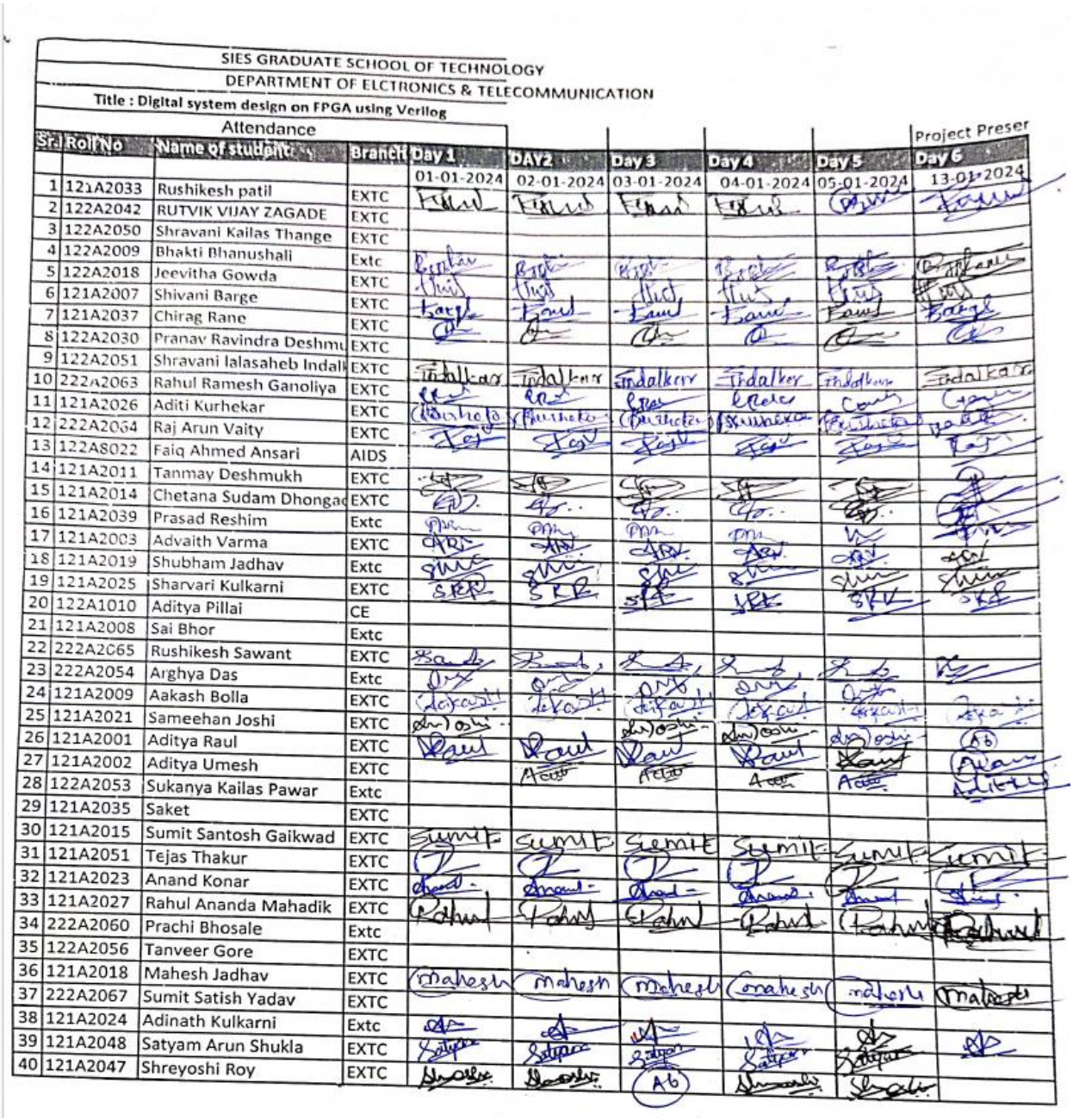
1. **List of Students :**

Sr.No	Student name	Class-Department (e.g. SE-ECS)	project title
1	Raj Vaity	TE-EXTC	CAR PARKING SLOT SYSTEM using FPGA
2	Rushikesh Sawant	TE-EXTC	CAR PARKING SLOT SYSTEM using FPGA
3	Rahul Ganoliya	TE-EXTC	CAR PARKING SLOT SYSTEM using FPGA
4	Arghya Das	TE-EXTC	CAR PARKING SLOT SYSTEM using FPGA
5	Shivani Barge	TE-EXTC	Design 2 bit carry look ahead adder using FPGA

6	Chirag Rane	TE-EXTC	Design 2 bit carry look ahead adder using FPGA
7	Advaith Varma	TE-EXTC	Traffic Light Controller using FPGA
8	Shubham Jadhav	TE-EXTC	Traffic Light Controller using FPGA
9	Sumit Gaikwad	TE-EXTC	Precision Demultiplexing: Building a 4-Channel Breakdown System
10	Mahesh Jadhav	TE-EXTC	Precision Demultiplexing: Building a 4-Channel Breakdown System
11	Rahul Mahadik	TE-EXTC	Precision Demultiplexing: Building a 4-Channel Breakdown System
12	Rushikesh patil	TE-EXTC	Coffee Vending Machine using FPGA
13	Shravani Indalkar	TE-EXTC	Coffee Vending Machine using FPGA
14	Bhakti Bhanushali	TE-EXTC	Coffee Vending Machine using FPGA
15	Jeevitha Gowda	TE-EXTC	Coffee Vending Machine using FPGA
16	Aditi Kurhekar	TE-EXTC	Pulse width modulation using FPGA
17	Tanmay Deshmukh	TE-EXTC	Pulse width modulation using FPGA
18	Chetana Sudam Dhongade	TE-EXTC	Pulse width modulation using FPGA
19	Sharvari Kulkarni	TE-EXTC	Pulse width modulation using FPGA
20	Aakash Bolla	TE-EXTC	Voting Machine using FPGA
21	Sameehan Joshi	TE-EXTC	Voting Machine using FPGA
22	Aditya Raul	TE-EXTC	Voting Machine using FPGA
23	Aditya Umesh	TE-EXTC	Voting Machine using FPGA
24	Tejas Thakur	TE-EXTC	Pulse width modulation using FPGA
25	Anand Konar	TE-EXTC	Pulse width modulation using FPGA
26	Sumit Satish Yadav	TE-EXTC	Pulse width modulation using FPGA
27	Adinath Kulkarni	TE-EXTC	Pulse width modulation using FPGA

28	Satyam Arun Shukla	TE-EXTC	Programmable digital delay timer
29	Shreyoshi Roy	TE-EXTC	Programmable digital delay timer

2. **Attendance report :**



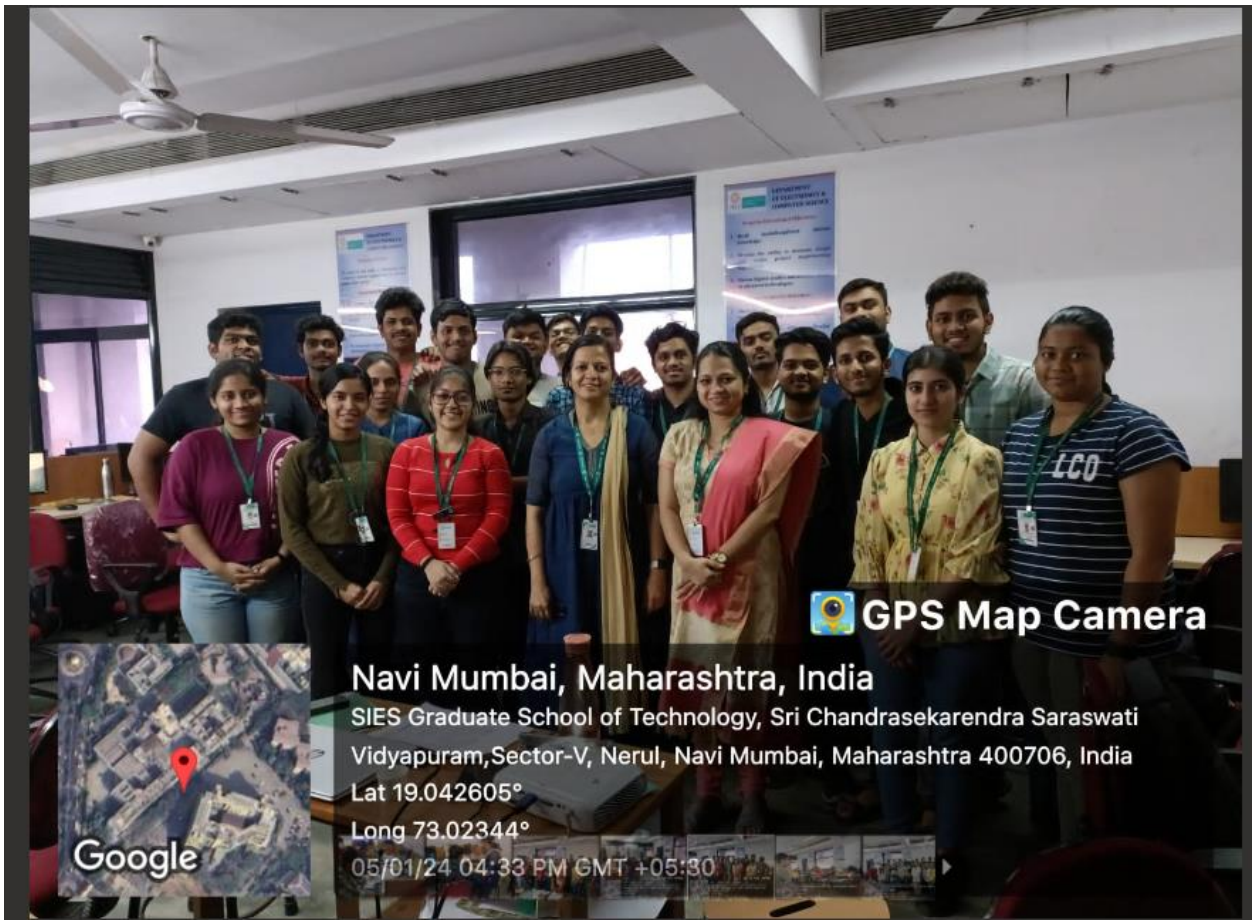
SIES GRADUATE SCHOOL OF TECHNOLOGY
DEPARTMENT OF ELCTRONICS & TELECOMMUNICATION
Title : Digital system design on FPGA using Verilog
Attendance

Sr.	Roll No	Name of student	Branch	Day 1	DAY2	Day 3	Day 4	Day 5	Project Preser Day 6
				01-01-2024	02-01-2024	03-01-2024	04-01-2024	05-01-2024	13-01-2024
1	121A2033	Rushikesh patil	EXTC						
2	122A2042	RUTVIK VIJAY ZAGADE	EXTC						
3	122A2050	Shravani Kailas Thange	EXTC						
4	122A2009	Bhakti Bhanushali	Extc						
5	122A2018	Jeevitha Gowda	EXTC						
6	121A2007	Shivani Barge	EXTC						
7	121A2037	Chirag Rane	EXTC						
8	122A2030	Pranav Ravindra Deshmu	EXTC						
9	122A2051	Shravani lalasaheb Indalk	EXTC						
10	222A2063	Rahul Ramesh Ganoliya	EXTC						
11	121A2026	Aditi Kurhekar	EXTC						
12	222A2064	Raj Arun Vaity	EXTC						
13	122A8022	Faiq Ahmed Ansari	AIDS						
14	121A2011	Tanmay Deshmukh	EXTC						
15	121A2014	Chetana Sudam Dhongad	EXTC						
16	121A2039	Prasad Reshim	Extc						
17	121A2003	Advaith Varma	EXTC						
18	121A2019	Shubham Jadhav	Extc						
19	121A2025	Sharvari Kulkarni	EXTC						
20	122A1010	Aditya Pillai	CE						
21	121A2008	Sai Bhor	Extc						
22	222A2065	Rushikesh Sawant	EXTC						
23	222A2054	Arghya Das	Extc						
24	121A2009	Aakash Bolla	EXTC						
25	121A2021	Sameehan Joshi	EXTC						
26	121A2001	Aditya Raul	EXTC						
27	121A2002	Aditya Umesh	EXTC						
28	122A2053	Sukanya Kailas Pawar	Extc						
29	121A2035	Saket	EXTC						
30	121A2015	Sumit Santosh Gaikwad	EXTC						
31	121A2051	Tejas Thakur	EXTC						
32	121A2023	Anand Konar	EXTC						
33	121A2027	Rahul Ananda Mahadik	EXTC						
34	222A2060	Prachi Bhosale	Extc						
35	122A2056	Tanveer Gore	EXTC						
36	121A2018	Mahesh Jadhav	EXTC						
37	222A2067	Sumit Satish Yadav	EXTC						
38	121A2024	Adinath Kulkarni	Extc						
39	121A2048	Satyam Arun Shukla	EXTC						
40	121A2047	Shreyoshi Roy	EXTC						

3. **Feedback**

Id	Name	Are you able to understand Sequential circuit execution?	Are you able to understand FSM executior	Content Delivery by Speakers	How relevant you think it was for your futu	Effectiveness of SDP	Satisfaction in general	Any other suggestion or Your views about SDP
1	JEEVITHA GOWDA	5	5	5	5	4	4	.
2	Sharvari Kulkarni	3	4	5	5	5	5	The SDP can be for more than a week for better understanding and practice.
3	RAJ VAITY	5	5	5	5	5	5	Very interesting session
4	Shivani Barge	4	3	4	4	4	4	No comments
5	Chirag Rane	4	4	3	4	4	4	No comments
6	Aditi Kurhekar	4	4	4	4	4	4	It was a wonderful session. Each and every concept was taught with very much clarity
7	RAHUL GANOLIYA	5	5	5	5	5	5	It was one of the best sdp with one of the best teaching faculty
8	BHAKTI BHANUSH	4	4	4	4	4	4	No. Suggestions
9	Advait Varma	4	4	4	4	4	4	It was a very interactive session and got to learn about many things in FPGA...which can be used in near future
10	Aditya	3	3	5	3	2	3	no
11	Mahesh Jadhav	5	5	5	5	5	5	
12	Tanmay Deshmuk	5	5	5	5	5	5	No suggestions
13	SHRAVANI INDALK	4	5	5	4	4	4	.
14	Aditya Raul	5	4	4	4	4	4	Links for the resources to learn about the same should have been provided.
15	Shubham Jadhav	4	5	4	5	4	5	It was a great experience and learning opportunity for us.
16	Aakash Bolla	4	4	4	4	4	4	.
17	photographyclub	5	4	5	4	5	5	Thank you! learned alot.
18	Satyam Shukla	5	5	5	5	5	5	It was amazing !
19	Tejas Thakur	5	5	5	5	5	5	-
20	Chetana Dhongad	4	3	5	5	4	4	The SDP was helpful in understanding the basics of verilog programming.
21	Sumit Gaikwad	4	4	4	4	5	4	No

4. **Certificate, Photographs (in JPEG/PNG) :**


GPS Map Camera
Navi Mumbai, Maharashtra, India
SIES Graduate School of Technology, Sri Chandrasekarendra Saraswati Vidyapuram,Sector-V, Nerul, Navi Mumbai, Maharashtra 400706, India
Lat 19.042605°
Long 73.02344°
05/01/24 04:33 PM GMT +05:30
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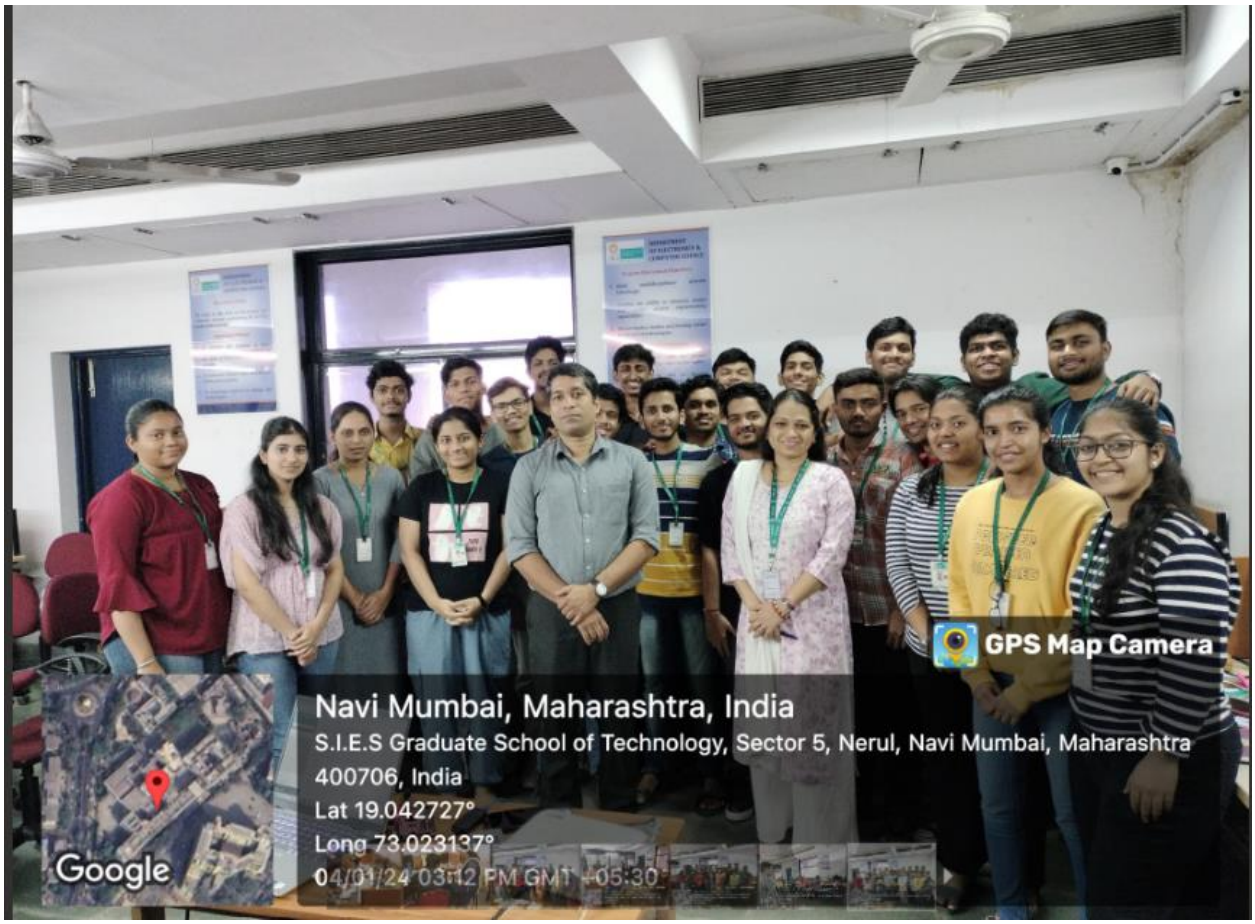

Quiz Result:

3. **Operator which precedes the operand** (1 point)
   69% of respondents (11 of 16) answered this question correctly.

More Details Insights

Unary	11	✓
Binary	3	
Ternary	0	
None	2	

4. **What is the time period of clock #10 clock = ~clock** (1 point)
31% of respondents (5 of 16) answered this question correctly.

More Details

10	10	
20	5	✓
5	1	
10	10	

5. **#40 $finish indicates** (1 point)
69% of respondents (11 of 16) answered this question correctly.

More Details Insights

end of simulation time	3	
end of simulation at 40 time units	11	✓
suspend simulation at 40 time u...	2	
None	0	

6. **What are the possible values of == operator** (1 point)
31% of respondents (5 of 16) answered this question correctly.

More Details

0,1	9	
0,x	0	
x	2	
0,1,x	5	✓

Certificate :